Automatic Impedance Matching for 13.56 MHz NFC Antennas

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Outline

1. Overview of the NFC Research Lab

2. Motivation
   - NFC Equipment and its Antennas
   - Impedance Matching

3. Automatic Impedance Matching
   - Automatic Tuning System
   - Measuring Circuit
   - Matching Circuit
   - Controller
   - Results

4. Summary and Outlook
Overview of the NFC Research Lab

NFC Research Lab

- Part of the R&D department of the Upper Austria University of Applied Sciences
- Funded by the BMVIT (Federal Ministry for Transport, Innovation and Technology) and FFG (Austrian Research Promotion Agency)
- We are focusing on
  - NFC hardware development
  - interoperability and performance testing for NFC systems
  - implementation of NFC applications
  - secure aspects for NFC systems and applications
- 1st Austrian NFC Trial
- Annual NFC Congress in Hagenberg
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NFC Equipment and its Antennas

- NFC transmission module IC has external antenna
- Mobile devices have though space-saving requirements
- Non-standard antennas necessary to fit casings
  - antennas have varying characteristics (shape, impedance)
  - each antenna has a certain impedance measured at its clamps
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What is Impedance Matching?

- Antenna’s impedance is the NFC IC’s load resistance
- 2 parameters depend on the NFC IC’s load resistance
  - the transmitter supply current and
  - the emitted RF power
- Both parameters decrease with increasing load resistance

- Good trade-off between both parameters around 40 to 50 ohms
**NFC Antenna Topology**

- NFC antenna topology with EMC filter, matching circuit, quality factor damping resistors and antenna coil
- $C_1$ and $C_2$ are adjusted until the whole topology circuit matches 50 ohms at its clamps (TX1, TX2)
Disadvantages of Manual Impedance Matching

- Expensive equipment (network analyzer, impedance analyzer)
- Time-consuming procedure
- Good sense of choosing the right capacitor values necessary
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Requirements

- Most NFC devices are mobile handsets
- Automatic tuning system must be small in shape and size
- Single chip solution preferred

⇒ ideal solution has only integrable parts
System Design

Automatic tuning system design split into its three components: measuring circuit, matching circuit and controller component.
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Wheatstone bridge with 13.56 MHz sinusoidal supply

Bridge is balanced ($V_{diff} = I_2 \cdot R_2 - I_Z \cdot Z = 0 V$)

⇒ Tuning circuit is matched to 50 ohms (at the operating frequency)
Balancing the Amplitude of $V_{\text{diff}}$

- Measuring rectifiers are used to rectify
  
  \[ V_{\text{SINE}1} = I_2 \cdot R_2 \text{ and } \]
  \[ V_{\text{SINE}2} = I_Z \cdot Z \]

- Resulting signals are low pass filtered

- $V_{\text{diff}}$ is calculated in software after analog-digital conversion
Balancing the Phase of $V_{\text{diff}}$

- $V_{\text{SINE1}}$ and $V_{\text{SINE2}}$ shaped into rectangular signals
- Phase detector: phase-offset is converted into a pulse-width modulated signal
- PWM signal is low pass filtered and fed into an analog-digital converter
Verification of the Measuring Circuit

- Verified with a manually tunable antenna circuit
- The antenna is connected to the measuring circuit and tuned
- Tuning is verified with a network analyzer
- Result is approximately the same with several tested antennas:
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Matching Circuit

- $C_1$ and $C_2$ in the antenna topology are replaced with capacitance arrays.
- Capacitance array: network of parallel switched capacitors.
- Capacitors switched with low-capacitance DMOS switches.

![Matching Circuit Diagram]
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Controller

- Analyses the measurands by reading the values from analog-digital converter
- Controls the capacitance arrays
- Tuning algorithm to minimize the amplitude and phase of $V_{\text{diff}}$ by optimal adjustment of $C_1$ and $C_2$
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Automatic Tuning Results

Antenna 1

Antenna 2

Antenna 3

Antenna 4
Automatic impedance matching significantly simplifies the integration of NFC ICs into applications. This automatic tuning system successfully finds the optimum values for the antenna circuit’s tuning capacitors. Only integrable components are used.

Outlook
- Parasitic effects of the DMOS switches need to be investigated.
- The tuning algorithm may be optimized.
- The whole system should be integrated into a single IC.